WHAT IS CLAIMED IS:

1. An integrated circuit (IC) output stage protection system, comprising:

a relatively low voltage CMOS device, having a gate configured to be coupled to an output of an IC logic core and a source coupled to a current source;

a first relatively high voltage CMOS device, having a source coupled to a drain of said relatively low voltage CMOS device and a gate coupled to a biasing circuit that biases said first relatively high voltage CMOS device so that said relatively low voltage CMOS device operates in a saturation region; and

one or more diodes coupled between an output node and a gate of a second relatively high voltage CMOS device, having a source coupled to a drain of said first relatively high voltage CMOS device and a drain coupled to said output node, wherein said one or more diodes substantially protect said CMOS devices so that they operate within a device voltage rating.

2. The IC output stage protection system of claim 1, wherein said one or more diodes are coupled to said gate of said second relatively high voltage CMOS device through a resistor.

3. The IC output stage protection system of claim 1, wherein at least one of said one or more diodes comprises a CMOS device configured as a diode,

said CMOS device having a guard ring coupled to first and second contacts on a P-substrate.

4. The IC output stage protection system of claim 1, further comprising:

an input/output (I/O) pad electrostatic discharge (ESD) protection circuit coupled to said output node.

5. The IC output stage protection system of claim 4, wherein said I/O pad ESD protection circuit comprises:

a first set of one or more diodes coupled between an I/O pad and a local net;

a second set of one or more diodes coupled between a ground and said I/O pad;

a CMOS device having a drain coupled to said local net, a source coupled to said ground, and a gate coupled to an output of an inverter;

a first resistor coupled between said local net and an input of said inverter;

a capacitor coupled between said input of said inverter and said ground; and

a second resistor coupled between said local net and said ground.

6. An integrated circuit (IC) output stage protection system, comprising:

a pair of relatively low voltage CMOS devices, each having a gate configured to be coupled to respective IC logic core outputs and a source coupled to a current source;

a first pair of relatively high voltage CMOS devices, each having a source coupled to a respective drain of said pair of relatively low voltage CMOS devices and a gate coupled to a biasing circuit that biases said first pair so that said pair of relatively low voltage CMOS devices operate in a saturation region;

a second pair of relatively high voltage CMOS devices, each having a source coupled to a respective drain of said first pair of relatively high voltage CMOS devices and a drain coupled to first and second output nodes, respectively;

a first set of one or more diodes coupled between said first output node and respective gates of said second pair of relatively high voltage CMOS devices; and

a second set of one or more diodes coupled between said second output node and said respective gates of said second pair of relatively high voltage CMOS devices;

wherein said first and second sets of one or more diodes substantially protect said CMOS devices so that they operate within a device voltage rating.

7. The IC output stage protection system of claim 6, wherein said first and second sets of one or more diodes are coupled to said respective gates of said second pair of relatively high voltage CMOS devices through a resistor.

8. The IC output stage protection system of claim 6, wherein:

said pair of relatively low voltage CMOS devices comprises a pair of relatively thin oxide devices; and

said first and second pairs of relatively high voltage CMOS devices comprise a first and second pair of relatively thick oxide devices.

9. The IC output stage protection system of claim 6, wherein said first and second sets of one or more diodes each comprise two diodes.

10. The IC output stage protection system of claim 6, wherein at least one of said diodes comprises a CMOS device configured as a diode, said CMOS device having a guard ring coupled to first and second contacts on a P-substrate.

11. The IC output stage protection system of claim 6, further comprising:

a first input/output (I/O) pad electrostatic discharge (ESD) protection circuit coupled to said first output node; and

a second I/O pad ESD protection circuit coupled to said second output node.

12. The IC output stage protection system of claim 11, wherein said first and second I/O pad ESD protection circuits each comprise:

a first set of one or more diodes coupled between an I/O pad and a local net;

a second set of one or more diodes coupled between a ground and said I/O pad;

a CMOS device having a drain coupled to said local net, a source coupled to said ground, and a gate coupled to an output of an inverter;

a first resistor coupled between said local net and an input of said inverter;

a capacitor coupled between said input of said inverter and said ground; and

a second resistor coupled between said local net and said ground.

13. An integrated circuit (IC) output stage protection system, comprising:

first and second input/output (I/O) pad electrostatic discharge (ESD) protection circuits coupled to respective first and second output nodes; and

an output stage, including:

first and second relatively low voltage CMOS devices having respective gates configured to be coupled to first and second IC core outputs, respectively, and respective sources coupled to a current source,

first and second relatively high voltage CMOS devices having respective sources coupled to respective drains of said first and second relatively low voltage CMOS devices and respective gates coupled to a biasing circuit,

third and fourth relatively high voltage CMOS devices having respective sources coupled to respective drains of said first and second relatively high voltage CMOS devices and respective drains coupled to first and second output nodes, respectively,

a first set of one or more diodes coupled between said first output node and respective gates of said third and fourth relatively high voltage CMOS devices, and

a second set of one or more diodes coupled between said second output node and said respective gates of said third and fourth relatively high voltage CMOS devices;

wherein said output stage protection system substantially protects said CMOS devices so that they operate within a device voltage rating during IC power up/power down and ESD events.

14. The IC output stage protection system of claim 13, wherein said first and second sets of one or more diodes are coupled to said respective gates of said third and fourth relatively high voltage CMOS devices through a resistor.

15. The IC output stage protection system of claim 13, wherein said first and second sets of one or more diodes each comprise two diodes.

16. The IC output stage protection system of claim 13, wherein at least one of said diodes comprises a CMOS device configured as a diode, said CMOS device having a guard ring coupled to first and second contacts on a P-substrate.

17. The IC output stage protection system of claim 13, wherein

said first and second relatively low voltage CMOS devices each comprise a 1.2 V device; and

said first, second, third, and fourth relatively high voltage CMOS devices each comprise a 2.5 V device.

18. The IC output stage protection system of claim 17, wherein a voltage difference between any two terminals of said first and second relatively low voltage CMOS devices does not exceed approximately 1.32 V, and wherein a voltage difference between any two terminals of said first, second, third, and fourth relatively high voltage CMOS devices does not exceed approximately 2.75 V.

19. The IC output stage protection system of claim 17, wherein said biasing circuit biases said gates of said first and second relatively high voltage

CMOS devices so a drain voltage of said first and second relatively low voltage CMOS devices does not exceed approximately 1.2 V.

20. The IC output stage protection system of claim 13, wherein said first and second I/O pad ESD protection circuits each comprise:

a first set of one or more diodes coupled between an I/O pad and a local net;

a second set of one or more diodes coupled between a ground and said I/O pad;

a CMOS device having a drain coupled to said local net, a source coupled to said ground, and a gate coupled to an output of an inverter;

a first resistor coupled between said local net and an input of said inverter;

a capacitor coupled between said input of said inverter and said ground; and

a second resistor coupled between said local net and said ground.